

What is claimed is:

1. A field effect transistor in which at least one vertically aligned semiconductor column (2) of a diameter in the nanometer range is present between a source electrode and a drain electrode (1, 7) and is annularly surrounded by a gate electrode with an insulating space between them,
characterized by the fact that
the semiconductor columns (2) are embedded in a first and a second insulating layer (3, 5) between which there is provided a metal layer (4) extending to the outside as a gate electrode whose ends penetrating through the second insulating layer (5) are partially converted to an insulator (6) or partially removed and filled by an insulating material.
2. A method of fabricating a field effect transistor in which at least one vertically aligned semiconductor column (2) of a diameter in the nanometer range is present between a source electrode and a drain electrode (1, 7) and is annularly surrounded by a gate electrode with an insulating space between them,
characterized by the fact that
 - free-standing semiconductor columns are grown vertically on a conductive substrate;
 - a first insulating layer is deposited on the semiconductor columns;
 - a first conductive metal layer and a second insulating layer are deposited thereon;
 - the developing laminates is etched planar to the point of the portion of the first metal layer covering the semiconductor columns is removed again;
 - the end of the metal layer penetrating to the surface of the laminate are etched back in a metal-specific manner and a third insulating layer is deposited on the laminate with subsequent

renewed planar etching;
or
the ends of the metal layer penetrating to the surface of the
laminate are converted to an insulator by oxidizing or nitriding;
5 and
- finally depositing a second metal layer on the laminate.

3. The method of claim 2,
characterized by the fact that
10 the laminate or individual layers are divided into individual arrays by a
lithographic process.

4. The method of claim 2,
characterized by the fact that
15 the growing of the semiconductor columns is carried out electro-chemically.

5. The method of claim 2,
characterized by the fact that
the growing of the semiconductor columns is carried out by sputtering.
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6. The method of claim 2,
characterized by the fact that
the growing of the semiconductor columns is carried out by a CVD process.

25 7. The method of claim 2,
characterized by the fact that
the growing of the semiconductor columns is carried out by vaporization.

8. The method of claim 2,
30 characterized by the fact that
the growing of the semiconductor columns is carried out in ion trace channels
of a polymeric film which is subsequently removed.